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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,919	04/16/2001	Hajime Akimoto	503.40029X00	5427

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EXAMINER	
KUMAR, SRILAKSHMI K	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/834,919	AKIMOTO ET AL.	
	Examiner	Art Unit	
	Srilakshmi K. Kumar	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,9,10,17,19,20,23,24 and 26-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9,10,17,19,20,23,24 and 26-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The following office action is in response to the Request for Continued Examination, filed on August 21, 2007. Claims 1-4, 9, 10, 17, 19, 20, 23, 24 and 26-28 are pending. Claims 1, 4, 9, 10, 17, 19, 23, 24 and 26-28 have been amended. Claims 5-8, 11-16, 18, 21, 22, 25 and 29-39 have been cancelled.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. ***Claims 1, 9,* 17, 23 and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriyama (US 5,583,533) in view of Yamaguchi et al. (U.S. Patent No. 5,627,557).

As to independent claim 1, Moriyama an image display apparatus (11) comprising; a plurality of signal lines (Fig. 8, item 11); a plurality of display pixels arranged in a matrix (col. 6, lines 16-19)) to provide image display, each of said display pixels (Fig. 8) comprising a pixel electrode (Fig. 8, item 13) connected to said each of the plurality of signal lines via a pixel switch (Fig. 8, item 14); a plurality of data lines (Fig. 8, item 12); a plurality of memory cells (Fig. 8, item 15) for storing digital display data (col. 6, lines 39-col. 7, line 8); an image signal generating circuit ( ) for outputting an image signal to the signal lines based on said digital display data inputted from the memory cells via the data lines (col. 15, lines 67-col.16, line 19);

Moriyama doesn't teach wherein each the plurality of memory cells comprises a memory switch; a memory capacitor connected to said memory switch and a field effect transistor of which a source drain path thereof is provided between a first node and a second node coupled to a corresponding one of said data lines, wherein one electrode of said memory capacitor is connected to a gate of said field effect transistor and another electrode of said memory capacitor is connected to said second node, and wherein when a memory cell is read or written, a predetermined voltage is supplied to said first node.

Yamaguchi et al teach wherein each the plurality of memory cells comprises a memory switch (1); a memory capacitor (CH) connected to said memory switch (Fig. 1, where 1 is connected to CH) and a field effect transistor (Fig. 2, item 2) of which a source drain path thereof is provided between a first node and a second node coupled to a corresponding one of said data lines (Fig. 2), wherein one electrode (top of CH) of said memory capacitor is connected to a gate of said field effect transistor and another electrode of said memory capacitor is connected to said

second node (CH) , and wherein when a memory cell is read or written, a predetermined voltage is supplied to said first node (Vee supplied to first node).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the configuration of the memory cells as taught by Yamaguchi into Moriyama et al in order to maintain a clear display for a long period of time and provide a display apparatus in which the degrading of the liquid crystal is prevented (Yamaguchi, col. 5, lines 16-28).

As to dependent claim 2, limitations of claim 1, and further comprising, Moriyama teaches wherein each of said plurality of display pixels is a liquid crystal display pixel having a counter electrode and a liquid crystal region between said pixel electrode and said counter electrode.

With reference to **claim 9,** Yamaguchi et al. teaches that the memory capacitor (CH) is a capacitor between a gate and a channel of the field effect transistor (see Figures 1-2).

With reference to **claim 17,** Yamaguchi et al teach wherein some of said memory cells are connected to one data line, and said second node is connected to said corresponding data line through a selection switch (1).

With reference to **claim 23,** Moriyama teaches wherein said memory cells are arranged in a matrix along said data lines extending in a y-direction (Fig 1), and said data lines are arranged by n line units in a case where unit digital display data composed of n bits is stored by n of said memory cells (Fig. 1, where the data lines and the memory cells correspond in number).

With reference to **claim 26,** Moriyama and Yamaguchi et al fail to specifically teach that the image signal generating means comprises a D/A converter. However, the Examiner takes

Official Notice that the usage of D/A converter is well known in the art for the data driver to include a D/A converter.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of a D/A converter for converting the digital data in to analog data for further image processing.

4. ***Claims 2, 3, 4, 20, 24, and 27*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriyama and Yamaguchi et al. as applied to **claims *1, 9,* 17, 23 and 26** above, and further in view of Parks (U.S. Patent No. 5,471,225).

With reference to **claims 2,** Moriyama and Yamaguchi et al. teach a liquid crystal display. Moriyama and Yamaguchi et al fail to specifically teach wherein each of the display pixels has a counter electrode and a liquid crystal region between said pixel electrode and said counter electrode.

Parks teaches the general construction of the LCD consisting of a pair of glass plates (22, 24), wherein the inside surface of glass panel (22) is a common electrode (30) and the inside of glass panel (24) is a pixel electrode wherein the liquid crystal (40) is located there between.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Park in Moriyama and Yamaguchi et al in order to provide an optimum display device which can be operated under a plurality of different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

With reference to **claim 3,** Moriyama and Yamaguchi et al also fail to teach that the plurality of display pixels have an optical reflecting plate.

Parks teaches that the usage of alignment coatings and/or passivity coatings, are generally placed between electrode (30) and liquid crystal medium (40) as well as between each display electrode and liquid crystal medium.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Park in Moriyama and Yamaguchi et al in order to provide an optimum display device which can be operated under a plurality of different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

With reference to **claim 4,** Yamaguchi et al. teaches that the LC panel (11) occupies a display portion including a scanning signal and data signal line driver can be included in the display portion as shift registers (14, 15) and timing generating circuit (17) (see column 16, lines 12-17) thereby reducing the area need for the components, and in turn allowing the display area to be made smaller.

With reference to **claims 20,** Yamaguchi et al. teaches with reference to conventional art that the switching elements are TFTs (see column 1, lines 8-17).

With reference to **claims 10**, Yamaguchi teaches that the memory capacitor (CH) is a capacitor between a gate and a channel of the amplifier (see Figures 1-2).

While Booth does teaches that the storage unit (124) may include a transistor that is activated to couple the capacitor to the pixel cell to refresh the terminal voltage across the pixel cell (see column 5, lines 33-38), the combination of Yamaguchi and Booth fail to teach that the switch or amplifier is of Poly-Si TFT type.

Parks teaches that the gate of the TFT is deposited upon the substrate accordingly to the well-known methods (see column 6, lines 36-52).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Yamaguchi et al., Booth, and Park in order to provide an optimum display device which can be operated under a plurality of different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

With reference to **claim 24,** Moriyama and Yamaguchi et al fail to specifically teach a black matrix shielding means arranged between the transparent substrate corresponding to the back portions of the memory element and a lighting means. However, the Examiner takes Official Notice that the usage of a black matrix is well known in the art.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of a black matrix in a device similar to that which is taught by the combination of Yamaguchi et al., Booth, and Parks in order to block unwanted light and thereby improving the contrast ratio of the display.

With reference to **claim 27**, Moriyama and Yamaguchi et al fail to specifically teach that the image signal generating means comprises a D/A converter. However, the Examiner takes Official Notice that the usage of D/A converter is well known in the art for the data driver to include a D/A converter.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of a D/A converter for converting the digital data in to analog data for further image processing.

5. ***Claims 10, 19 and 28*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriyama in view of Zhang et al. (U.S. Patent No. 6,611,261).

With reference to **claim 28**, Moriyama teaches an image display apparatus comprising; a plurality of display pixels arranged in a matrix in order to provide image display (col. 6, lines 16-19), each display pixel comprising a pixel electrode (Fig. 8, item 13) and a pixels switch connected to said pixel electrode in series (Fig. 8, item 14), a group of signal lines (Fig. 8, item 11) and display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches (col. 15, lines 67-col. 16, lines 30)

Moriyama doesn't teach a digital to analog converter and where the D-to-A converter contains a reference voltage generating circuit using a boron doped poly-Si thin film resistor as a gray scale voltage generating resistor.

Zhang et al. teaches a LCD device wherein it is disclosed the conventionality of using poly-silicon thin film transistors in LCD units and the peripheral circuits as well (see column 1, lines 15-20). It is further taught the usage of a D/A converter (350), which is comprised in the poly-Si digital driver, for generating gray scale signals based on the gray-scale reference voltage (see column 15, lines 42-57).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the combination of the poly-Si type image signal generating means as taught by Zhang et al. to be used in a device similar to that which is taught by Moriyama in order to provide an improved arrangement for peripheral circuits of the display unit thereby allowing them to be formed as an integrated device.

6. ***Claims 10 and 19*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriyama and Yamaguchi et al. as applied to claims ***1, 9,*** **17, 23 and 26** and further in view of Zhang et al. (U.S. Patent No. 6,611,261).

With respect to claims 10 and 19, see rejection of claim 28 above.

Response to Arguments

Applicant's arguments with respect to claims 1-4, 9, 10, 17, 19-20, 23, 24, 26-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 571 272 7769. The examiner can normally be reached on 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Lefkowitz can be reached on 571 272 3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Srilakshmi K Kumar
Examiner
Art Unit 2629

SKK
November 7, 2007